AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A CCD pulse generator comprising:

a digital delay type CCD control signal generating section ~~means~~ for finely delaying a transfer signal for driving a CCD, thereby generating a plurality of delay signals, and changing selection of the plurality of delay signals, thereby generating a CCD control signal corresponding to set rise and fall timings;

an inverted/non-inverted signal generating section ~~means~~ for generating an inverted signal and a non-inverted signal of the CCD control signal;

a selection section ~~means~~ for selecting the inverted signal and the non-inverted signal of the CCD control signal;

an output section ~~means~~, having an output enable function, for outputting the signal selected by said selection section ~~means~~; and

an output signal condition setting section ~~means~~ for setting pieces of condition setting information that determine operations of said respective sections, said output signal condition setting section being formed by a register which is controlled by data, clock, and load control signals.

2. (Currently Amended) [[A]] The generator according to claim 1, wherein the CCD pulse generator further comprises a blanking section ~~means~~ for temporarily

disabling a CCD reset signal, [[and]] wherein the CCD control signal includes the CCD reset signal.

3. (Currently Amended) [[A]] The generator according to claim 1, wherein the CCD pulse generator further comprises a blanking section ~~means~~ for temporarily disabling a CCD clamp signal, [[and]] wherein the CCD control signal includes the CCD clamp signal.

4. (Currently Amended) [[A]] The generator according to claim 1, wherein the CCD pulse generator further comprises a blanking section ~~means~~ for temporarily disabling a CCD spare signal, [[and]] wherein the CCD control signal includes the CCD spare signal.

5. (Currently Amended) [[A]] The generator according to claim 1, wherein the CCD control signal includes a CCD spare signal.

6. (Currently Amended) [[A]] The generator according to claim 5, further comprising a blanking section ~~means~~ for temporarily disabling the CCD spare signal.

7. (Currently Amended) A CCD pulse generator comprising:

a digital delay type sampling signal generating section ~~means~~ for finely delaying a transfer signal for driving a CCD, thereby generating a plurality of delay signals, and

changing selection of the plurality of delay signals, thereby generating a sampling signal for sampling a CCD output in synchronism with set rise and fall timings;

an inverted/non-inverted signal generating section ~~means~~ for generating an inverted signal and a non-inverted signal of the CCD control signal;

a selection section ~~means~~ for selecting the inverted signal and the non-inverted signal of the CCD control signal;

an output section ~~means~~, having an output enable function, for outputting the signal selected by said selection section ~~means~~; and

an output signal condition setting section ~~means~~ for setting pieces of condition setting information that determine operations of said respective sections, said output signal condition setting section being formed by a register which is controlled by data, clock, and load control signals.

8. (Canceled)

9. (Currently Amended) [[A]] The generator according to claim 1 [[8]], wherein said output signal condition setting section ~~means is formed by a register which is controlled by three data, clock, and load control signals, and~~ can be cascade-connected to another functional element section ~~means~~ formed by a register which is controlled by data, clock, and load control signals.

10. (Currently Amended) [[A]] The generator according to claim 1 [[8]], wherein the register is controlled via a terminal for selecting an element operation order.

11. (Currently Amended) [[A]] The generator according to claim 1 [[8]], wherein the register is controlled via a terminal for element enable selection.

12. (Currently Amended) [[A]] The generator according to claim 1 [[8]], wherein the register is controlled via communication by a setting section ~~means~~ including a CPU.

13. (Currently Amended) [[A]] The generator according to claim 1 [[8]], wherein said respective sections ~~means~~ are arranged in one chip of an integrated circuit.

14. (Currently Amended) [[A]] The pulse generator unit which is formed by combining at least two of pulse generators defined in claims 2 to 6 and comprises a plurality of output sections ~~means~~, wherein all output enable functions of said output sections ~~means~~ are simultaneously controlled by one setting.

15. (Currently Amended) [[A]] The generator according to claim 1, wherein the transfer signal is received by a differential input section ~~means~~ to generate the plurality of delay signals.

16. (Currently Amended) [[A]] The generator according to claim 2, wherein said respective sections ~~means~~ are arranged in one chip of an integrated circuit,

said blanking section ~~means~~ comprises an internal blanking signal generating section ~~means~~ for generating a blanking signal within the integrated circuit, an external blanking signal input section ~~means~~ for receiving a blanking signal outside the integrated circuit, and a blanking signal selection section ~~means~~ for selecting the internal blanking signal and the external blanking signal, and

selection of said blanking signal selection section ~~means~~ is set by said output signal condition setting section ~~means~~.

17. (Currently Amended) [[A]] The generator according to claim 1, wherein a signal for driving a line CCD is generated.

18. (Currently Amended) An image forming apparatus comprising:

a CCD;

a digital delay type CCD control signal generating section ~~means~~ for finely delaying a transfer signal for driving said CCD, thereby generating a plurality of delay signals, and changing selection of the plurality of delay signals, thereby generating a CCD control signal corresponding to set rise and fall timings;

an inverted/non-inverted signal generating section ~~means~~ for generating an inverted signal and a non-inverted signal of the CCD control signal;

a selection section ~~means~~ for selecting the inverted signal and the non-inverted signal of the CCD control signal;

an output section ~~means~~, having an output enable function, for outputting the signal selected by said selection section ~~means~~; and

an output signal condition setting section ~~means~~ for setting pieces of condition setting information that determine operations of said respective ~~means~~ sections, said output signal condition setting section being formed by a register which is controlled by three, data, clock, and load control signals.

19. (Currently Amended) [[A]] The apparatus according to claim 18, wherein the image forming apparatus further comprises a blanking section ~~means~~ for temporarily disabling a CCD reset signal, and

the CCD control signal includes the CCD reset signal.

20. (Currently Amended) [[A]] The apparatus according to claim 18, wherein the image forming apparatus further comprises a blanking section ~~means~~ for temporarily disabling a CCD clamp signal, and

the CCD control signal includes the CCD clamp signal.

21. (Currently Amended) [[A]] The apparatus according to claim 18, wherein the image forming apparatus further comprises a blanking section ~~means~~ for temporarily disabling a CCD spare signal, and

the CCD control signal includes the CCD spare signal.

22. (Currently Amended) [[A]] The apparatus according to claim 18, wherein the CCD control signal includes a CCD spare signal.

23. (Currently Amended) [[A]] The apparatus according to claim 22, further comprising a blanking section ~~means~~ for temporarily disabling the CCD spare signal.